AVOIDING CROSS TALK AND FEED BACK EFFECTS IN PACKAGING COPLANAR MILLIMETER-WAVE CIRCUITS

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***Abstract* - The impact of the packaging configuration on cross talk and feed back effects caused by parasitic substrate modes is investigated for coplanar millimeter-wave circuits. It is demonstrated theoretically and by means of several circuit examples that both the mounting configuration and the thickness of the semiconductor substrate of coplanar MMICs have to be chosen appropriately, in order to avoid circuit degradation or even failure.**

I. INTRODUCTION

It has been outlined by various authors that planar MMW circuits may suffer from parasitic modes due to power leakage from uniform transmission lines [1-4] and excitation at discontinuities [5, 6]. Clearly, the importance of these effects lies within the resulting undesired and often unexpected cross talk and feed back which is introduced to the circuit and can seriously degrade its performance. Since for coplanar MMICs, effects related to parasitic modes are essentially determined by the circuit backside and the thickness of the semiconductor substrate, they are in general a packaging problem.

In the work presented here, we examine the impact of the packaging configuration, including the mounting surface and the substrate thickness, on parasitic mode effects for coplanar MMICs. Also, we demonstrate how the enhanced cross talk and feed back resulting form parasitic modes affect the circuit performance.

On the one hand, we use high gain coplanar amplifiers, operating at W-band frequencies as practical circuit examples. Here, parasitic feed back, which is caused by propagating modes in the substrate, has a distinct influence on the circuit stability. This is demonstrated by means of the circuit gain and the stability factor μ.

On the other hand, the well established spectral domain approach is employed for theoretical explanation. The power leakage for the coplanar transmission lines used in the amplifier designs is calculated, and the leakage constant α serves as a measure for the parasitic coupling in the circuit. The different packaging configurations under investigation are the mounting on a metal package surface, the mounting on a dielectric carrier, and the flip chip technology.

II. MOUNTING ON METAL SURFACE

The mounting of coplanar MMICs on a metal package surface introduces a conductor backing and leads to parasitic parallel plate modes. The standard thickness of coplanar MMICs fabricated on 3 inch GaAs wafers is 25 mils. However, substrate thinning is quite often done prior to pack-

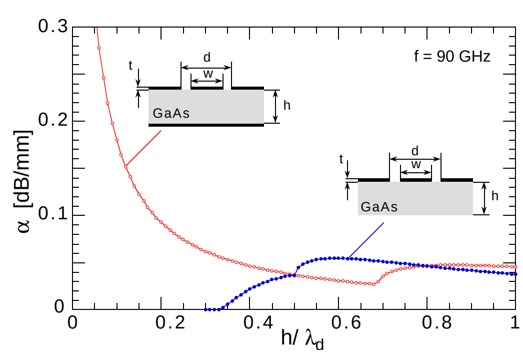

Fig. 1 Leakage constant α for coplanar transmission line vs. normalized substrate thickness (d = 50 µm, w = 17 µm, t = 3 µm, ε_r = 12.9, f = 90 GHz).

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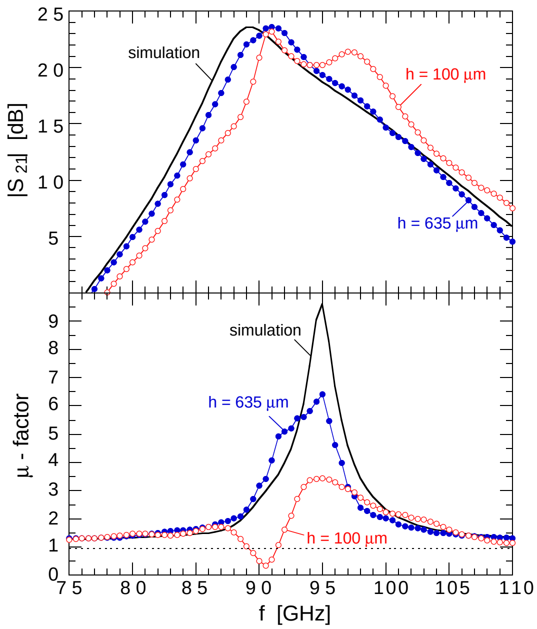

Fig. 2 Gain and μ-factor of two stage coplanar amplifier mouted on metal surface.

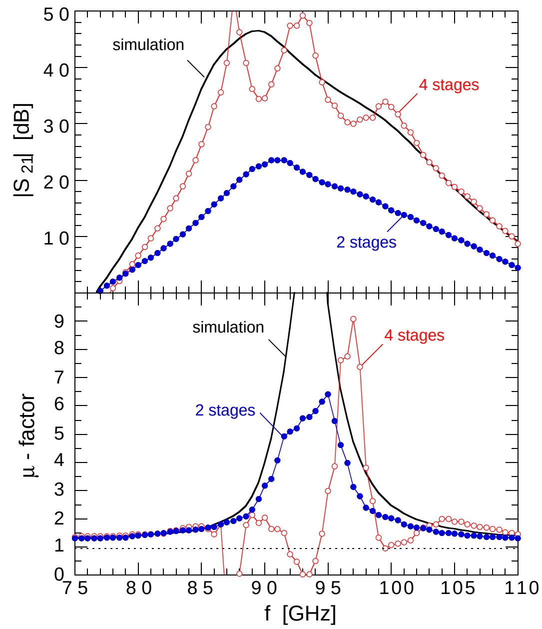

Fig. 3 Gain and μ-factor of two and four stage coplanar amplifier mounted on a metal surface (h = 635 µm).

aging to improve the heatsinking capability or to facilitate the combination with microstrip circuits within multichip modules. The effect of the GaAs substrate thickness h on the leakage constant α is shown in Fig. 1 for CPWs with d = 50 µm, as they are commonly used in our circuit designs. Evidently, for the conductor backed CPW a reduction of h from 635 µm ($h/\lambda_d = 0.69$ at 90 GHz) to 100 µm ($h/\lambda_d = 0.1$ at 90 GHz) corresponds to a drastic increase in power leakage.

A two stage cascode amplifier [7] is used as a circuit example to demonstrate the influence of the substrate thickness for conductor backed coplanar MMICs. The measured gain and μ-factor (which indicates unconditional circuit stability when it is greater than one) are shown in Fig. 2. While the circuit with h = 635 µm has a smooth gain curve with a maximum value of about 20 dB around 90 GHz and a μ-factor always greater than one, the thinned amplifier becomes unstable and its gain deviates strongly from the simulated performance. This instability is attributed to an enhanced internal feed back in the thinned conductor backed configuration.

III. MOUNTING ON DIELECTRIC CARRIER

The use of a dielectric carrier between the MMIC and the package surface has been proposed to reduce the impact of parasitic modes [3].

The circuit chosen to investigate this effect is a four stage amplifier which consists of two cascaded 2-stage amplifiers [8]. Fig. 3 shows the measured gain and μ-factor for the two and the four stage amplifier with a conductor backing present. It can be noticed that due to the increased gain, the four stage amplifier is already highly unstable on a conductor backed full thickness chip.

Fig. 4 shows the influence a 2 mm thick dielectric carrier underneath the MMIC has on the leakage constant α for the CPWs used in the amplifier circuit. The graph reveals that for the standard GaAs thickness of h = 635 µm, the dielectric constant of the carrier has almost no influence,

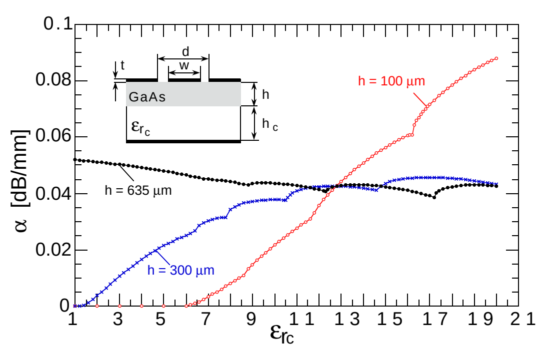

Fig. 4 Leakage constant α for CPW on GaAs and dielectric carrier vs. dielectric constant of carrier (d = 50 µm, w = 17 µm, t = 3 µm, ε_r = 12.9, h_c = 2 mm and f = 90 GHz).

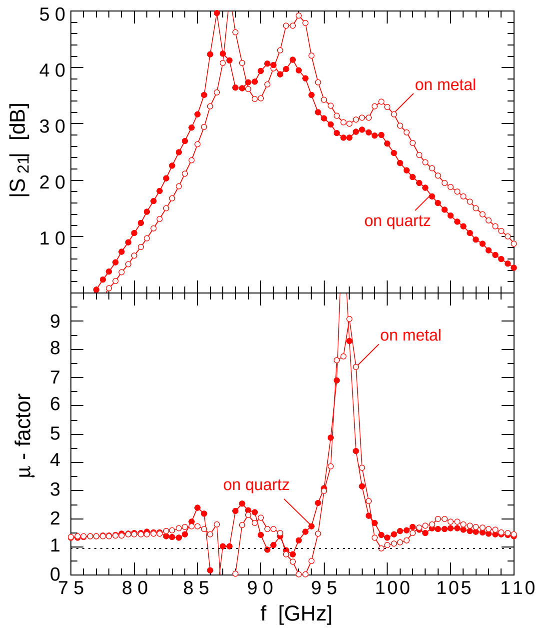

Fig. 5 Gain and μ-factor of four stage coplanar amplifier mounted on a metal surface or an additional quartz carrier with ε_{rc} = 3.8 and h_c = 2 mm. The thickness of the GaAs chips is h = 635 µm.

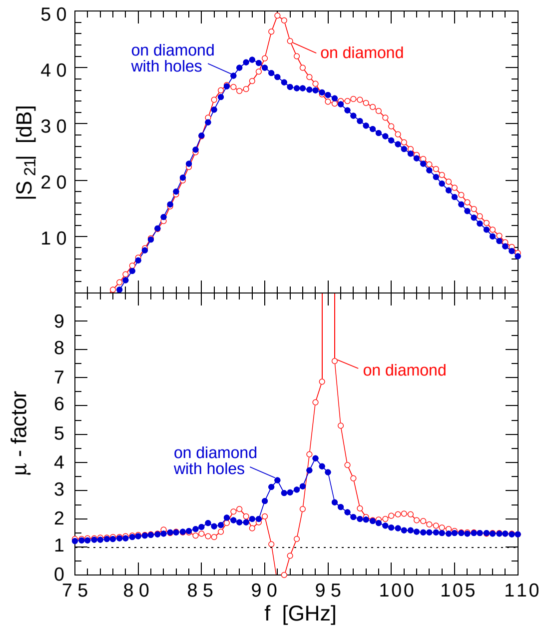

Fig. 7 Gain and μ-factor of four stage coplanar amplifier on diamond carrier (ε_{rc} = 5.8 and h_c = 0.3 mm) with and without laser drilled holes. The thickness of the GaAs chips is h = 100 µm.

and α is similar to the value for the conductor backed configuration in Fig. 1. This is confirmed experimentally by Fig. 5 where an additional quartz carrier is inserted between the four stage amplifier MMIC and the metal package surface. Clearly, no improvement is achieved.

However, Fig. 4 also shows that for a reduced chip thickness the use of a dielectric carrier with low ε_{rc} results in an improved leakage performance. A first experimental verification of this is given in Fig. 6. Here, the measured cross talk between two parallel CPWs on GaAs is shown using different substrate thicknesses and mounting surfaces. On the one hand, it can be seen that a similar cross talk is measured for the full thickness substrate regardless of the mounting surface. On the other hand, the measured cross talk is increased by substrate thinning in the conductor backed configuration and reduced when the additional quartz carrier is inserted.

As a carrier for the thinned 4-stage amplifier we have chosen diamond, which due to its excellent thermal conductivity is more suited for MMIC mounting than quartz. However, as Fig. 7 shows, the available material with ε_{rc} = 5.8 and h_c = 0.3 mm was not sufficient to achieve the required unconditionally stable operation of the amplifier. Therefore, ε_{rc} is artificially lowered by

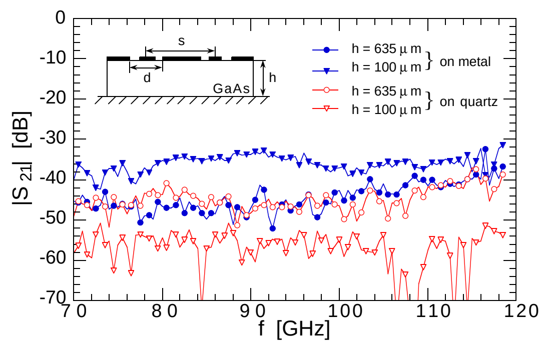

Fig. 6 Measured cross talk between parallel CPWs on GaAs (d = 50 µm, w = 17 µm, t = 3 µm, s = 750 µm).

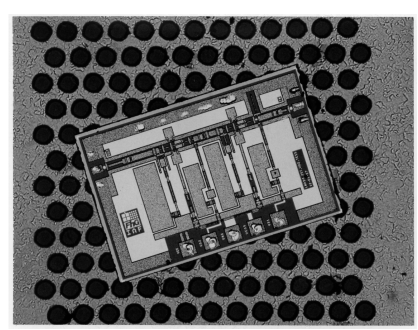

Fig. 8 Coplanar MMW-amplifier on diamond substrate with laser drilled holes.

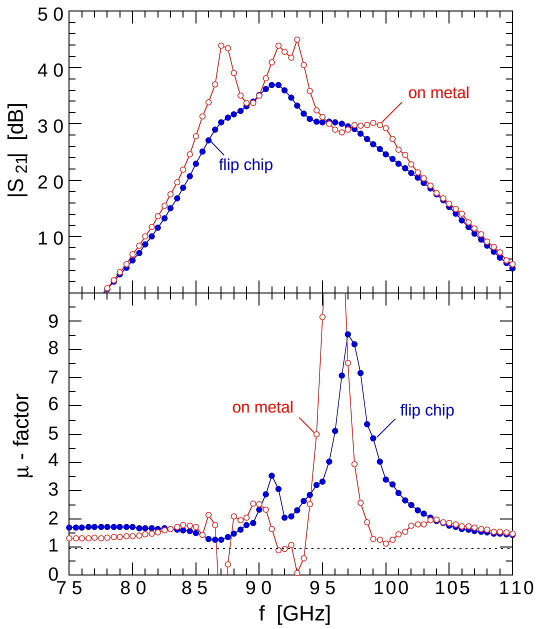

Fig. 9 Gain and µ-factor of thinned four stage coplanar amplifier in flip chip configuration (h = 100 µm). And performance before thinning (h = 635 µm) on metal surface.

laser drilling holes in the diamond [9]. The resulting packaging configuration is shown in Fig. 8. The amplifier performance in this packaging configuration is also shown in Fig. 7. A stable operation with a peak gain of over 40 dB around 90 GHz is achieved.

III. FLIP CHIP MOUNTING

As another promising packaging approach flip chip mounting of the four stage amplifier was performed [10] (Fig. 10). Here the circuit backside remains uncovered. According to Fig. 1, thinning of the GaAs substrate reduces power leakage into surface waves. Fig. 9 shows the gain and μ factor of the four stage amplifier measured on a thinned (h = 100 µm) and flip chip mounted MMIC. The required stable amplifier operation is achieved, and the improvement compared to the performance before thinning is obvious.

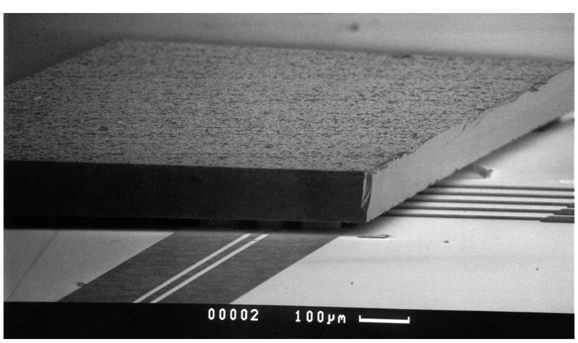

Fig. 10 Photo of four stage coplanar amplifier assembled in flip chip technology.

IV. ACKNOWLEDGMENT

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